CLAIMS

What is claimed is:

1. A differential transistor pair circuit having resistive load elements connected to collectors thereof, the improvement comprising:

an inductor coupled in series with each of the resistive load elements, such that the inductors are coupled to each other by mutual inductance.

- 2. The differential transistor pair circuit of Claim 1 where the inductors are connected out-of-phase at the collectors of the transistors.
 - 3. A differential circuit having a compound load, comprising:

 a differential pair of transistors having emitters coupled together;
 a load resistor coupled to a collector of each transistor; and
 an inductor coupled in series with each of the load resistors, where

 the inductors are magnetically coupled together.
- 4. The differential circuit of Claim 3 wherein the inductors are connected out-of-phase at the collectors of the transistors.
- 5. The differential circuit of Claim 3 further comprises a common current source connected to the emitters of the transistors.

- 6. The differential circuit of Claim 3 wherein a differential signal of opposite polarity is applied to bases of the transistors.
- 7. The differential circuit of Claim 3 further comprises a buffer stage operable to reduce loading of the collectors of the transistors.
- 8. A method for increasing bandwidth of a differential transistor pair circuit having resistive load elements connected to collectors thereof, comprising: connecting an inductor in series with each of the resistive load elements; and

magnetically coupling the inductors together.